CLAIMS

1. A signal processor comprising:

(1) a plurality of function blocks for signal processing; and

(2) a dedicated output path for transmitting debug information for debugging for the signal processor obtained from each of the plurality of function blocks.

2. The signal processor according to claim 1, wherein the dedicated output path transmits the debug information serially.

3. The signal processor according to claim 1, wherein the debug information includes input data to at least one of the plurality of function blocks.

4. The signal processor according to claim 1, wherein the debug information includes output data from at least one of the plurality of function blocks.

5. The signal processor according to claim 1, wherein the debug information is data in an arbitrary length (size).

6. The signal processor according to claim 1, wherein the signal processor is designed for a mobile communication system,

and

wherein one of the plurality of function blocks is an error correction coder block, which inputs transmission data for coding as input data, performs error correction coding as the signal processing, and outputs a coded data series as output data.

7. The signal processor according to claim 1, wherein the signal processor is designed for a mobile communication system, and

wherein one of the plurality of function blocks is a modulator block, which inputs a coded data series as input data, performs modulation as the signal processing, and outputs modulated transmission data as output data.

8. The signal processor according to claim 1, wherein the signal processor is designed for a mobile communication system, and

wherein one of the plurality of function blocks is a demodulator block, which inputs received modulated data as input data, performs demodulation as the signal processing, and outputs a demodulated data series as output data.

9. The signal processor according to claim 1, wherein the signal processor is designed for a mobile communication system, and

wherein one of the plurality of function blocks is an error correction decoder block, which inputs a decoded data series as input data, performs error bit correction as the signal processing, and outputs decoded data as output data.

10. The signal processor according to claim 1, further comprising:

a selection multiplex output block for acquiring an instruction from an outside, selecting the debug information based on the instruction acquired, inputting the debug information selected via the dedicated output path, and outputting the debug information inputted to the outside.

11. The signal processor according to claim 10, wherein the selection multiplex output block selects multiple pieces of debug information based on the instruction, inputs the multiple pieces of debug information, multiplexes the multiple pieces of debug information, and outputs multiplexed debug information to the outside.

12. The signal processor according to claim 11, wherein the multiple pieces of debug information are acquired from different function blocks.

13. The signal processor according to claim 10, wherein the

selection multiplex output block performs time multiplexing.

14. The signal processor according to claim 1, wherein the debug information is added with time information.

15. The signal processor according to claim 14, wherein the time information is added by a function block.

16. The signal processor according to claim 15, wherein the time information includes a plurality of frame counters of different cycles.

17. The signal processor according to claim 16, wherein the plurality of frame counters includes CFN (Connection Frame Number Counter) and BFN (Node B Frame Number Counter).